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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,224	08/26/2003	Hiroshi Seki	116652	1904

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EXAMINER	
CHANG, JOSEPH	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,224	SEKI, HIROSHI	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 6* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050428*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments with respect to claims1-6 have been considered but are moot in view of the new ground(s) of rejection. Examiner made a correction on the limitation "an inverter" in claim 1 as TR3-TR6 of Figure 2, not INV2 indicated in the previous Office Action.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A semiconductor device using an oscillator with a transmission gate and a clamping circuit.

The disclosure is objected to because of the following informalities: In the brief description of the drawings section, Paragraph [0021] describes incorrect information on Fig. 6. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura, US Patent No. 5,900,787 in view of Williams et al., US Patent No. 5,896,069 and Delhaye et al., US Patent No. 5,039,985.

Yoshimura discloses a semiconductor device (Fig.2) utilizing an oscillator (OSC0, OSC1) installed outside and having an inverting amplifier (Fig.2), which is installed in parallel with the oscillator (OSC0, OSC1 terminals are in parallel with the oscillator, not shown), the oscillator intermittently outputting an oscillation signal in response to a control signal (CONT), the inverting amplifier comprising:

a first terminal (OSC0) that receives a first signal from the oscillator;

a second terminal (OSC1) that provides a second signal to the oscillator;

a transmission gate (14) disposed between the first terminal and the second terminal, that is formed, the transmission gate being set to an 'on' state where the first signal is transmitted in a case of the control signal being set to a first logical level, and set to an 'off' state where the first signal is not transmitted in the other case of the control signal being set to a second logical level (the circuit structure inherently functions as recited);

an inverter (11, TR5 and TR6) disposed between an output terminal (upper node of 14) of the transmission gate (14) and the second terminal (OSC1), and inverting a logical level of a given signal so as to output the second signal (inverter's intrinsic functionality).

However, Yoshimura does not show a clamping circuit nor insulated gate transistors, the clamping circuit being disposed between the output terminal of the transmission gate and an input terminal of the inverter that is formed by using the insulated gate transistor, the clamping circuit being set to make the first signal output from the transmission gate applied to the input terminal of the inverter in a case of the

control signal being set to the first logical level, and set to make predetermined voltage applied to an input terminal of the inverter in the other case of the control signal being set to the second logical level.

Williams et al. discloses a claiming circuit (272, 274) and further discloses that the circuit provides improved immunity to process variation and power supply variation and improved noise insensitivity (Col. 3, lines 2-5).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the clamping circuit of Williams et al. in the Yoshimura circuit so as to dispose between the output terminal of the transmission gate and an input terminal of the inverter because such a modification would have provided the improved immunity to process variation and power supply variation and improved noise insensitivity as taught by Williams et al.

Regarding an insulated gate transistor, this type of transistor is well known in complementary metal oxide semiconductor (CMOS) construction. Delhaye et al. discloses an integrated semiconductor device including an insulated gate transistor and further discloses that the insulated gate transistor provides a negative conductance and an adjustable output power thus the output signal is more stable than that of known circuit (Col. 2, lines 33-35). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use an insulated gate transistor in the Yoshimura circuit because such a modification would have provided the benefits as taught by Delhaye et al.

Regarding Claim 2, Fig. 2 shows a CMOS transmission gate (14).

Regarding Claim 3, such a buffer would have been obvious based on the stability of the input and output stages.

Regarding Claim 5, such a feedback resistor would have been obvious based on the well-known configuration as shown in Figure 1 (R1).

Regarding Claim 6, an oscillator is necessarily present in the OSC0 and OSC1 described in the Fig.2.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Yoshimura, taken alone or in combination of other references, does not teach or fairly suggest a transmission gate that is disposed between the inverting amplifier and the buffer, and that is formed by using the insulated gate transistors.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Embree et al discloses a CMOS oscillator having insulated gate transistors.

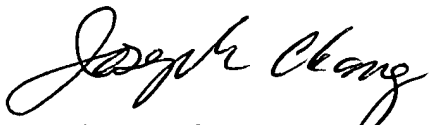
Kuo discloses a ring VCO having a clamping circuit.

JP 56016304A discloses a quartz oscillator having a clamping circuit between two amplifiers in the oscillator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph Chang
Patent Examiner
Art Unit 2817